Crystal Clear Technology

Product Specification

T2440W01B00

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1.0 Table of contents

2.0 Record of revision

Rev	Date	Item	Page	Comment	Originator	Checked By
1.0	12/12/13			Initial Release	Wai Hong	Azhar

3.0 General specification

Panel size: 4.8 inch

Display format: Graphics 400 (w) x 240 (h) dots

Dot pitch: 0.26 (w) x 0.26 (h) mm

Active area: 104.0 (w) x 62.4 (h) mm

General dimensions: 110.2 (w) x 73.7.0 (h) x 4.0 (t) mm

Color pixel arrangement: Mono stripe

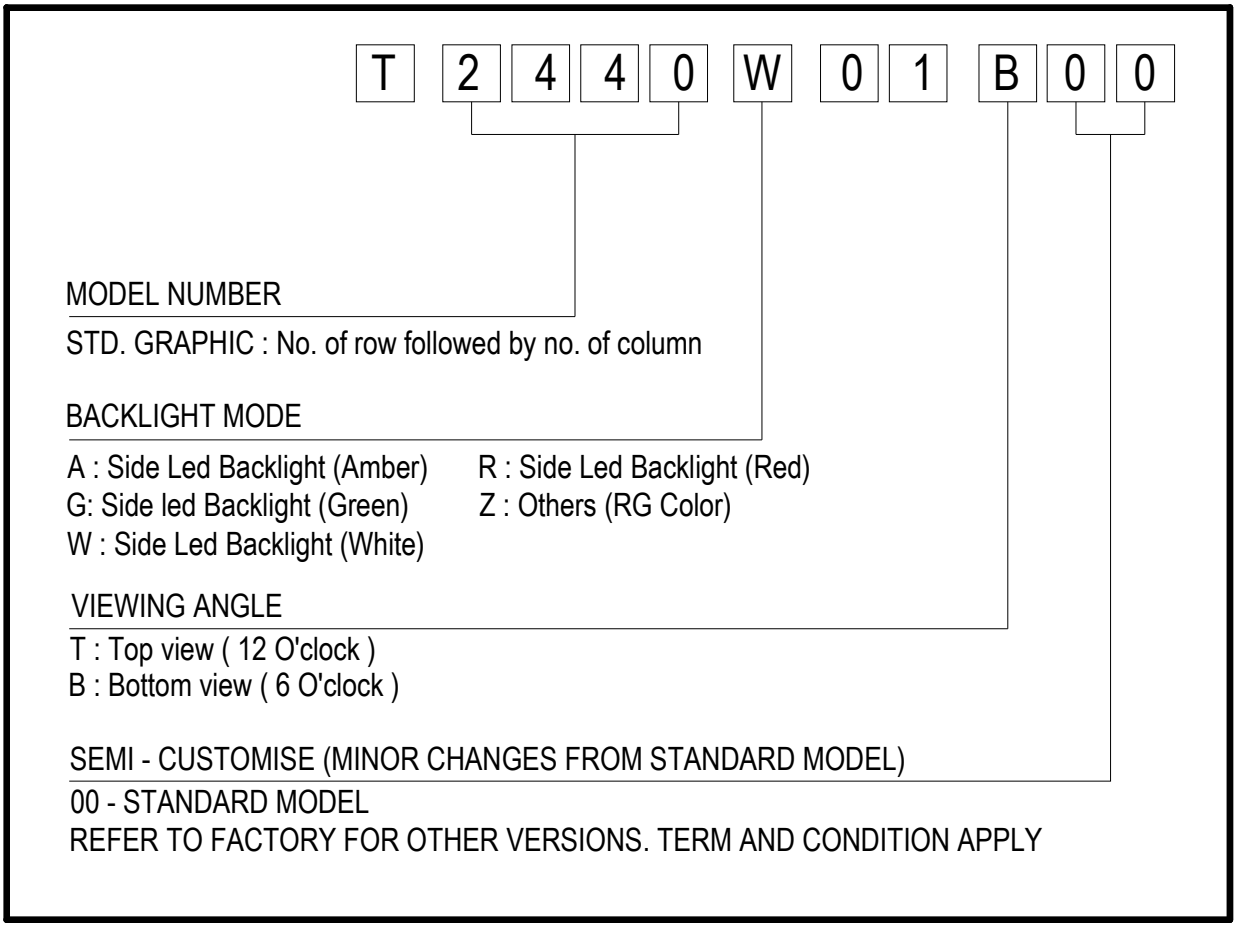
Display mode: Normal White

Driving method: TFT active matrix

Viewing direction: 6 O'clock

LCD controller / driver: ST7513 or equivalent

Interface: LCD controller / driver – Parallel 6800 / 8080, 4-line serial, 3-line serial



4.0 Absolute maximum rating (at Vss = 0V, ambient temperature = 25°C)

NO	ITEM	SIMBOL	MIN	MAX	UNIT
1.	Power Supply Voltage	VDDI, VDDA	- 0.3	6.0	V
2.	LCD Power Supply Voltage	AVDD, GVDD		7.0	V
		AVCL, GVCL, VCOM		- 7.0	V
		VGH - VGL		35.0	V
3.	MCU Interface Input Voltage	V_{IN}	- 0.3	VDDI+0.3	V
4.	Operating Temperature	T_{op}	-20°C to +70°C		°C
5.	Storage Temperature	T_{st}	-30°C to +80°C		°C

5.0 Electrical characteristics

NO	ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Operating Voltage	VDDI, VDDA	-	2.7	-	5.5	V
2.	Operating Voltage	VCCO	Built-in power	-	1.8	-	V
3.	Operating Voltage	GVDD	Built-in power	2.7	-	5.8	V
4.	Operating Voltage	GVCL	Built-in power	- 5.8	-	- 2.7	V
5.	Operating Voltage	VGH	Built-in power	8.0	-	19.0	V
6.	Operating Voltage	VGL	Built-in power	- 15.0	-	- 5.0	V
7.	Operating Voltage	VCOM	Built-in power	- 2.0	-	0.0	V
8.	“H” Input Voltage	V_{IH}	-	0.8VDDI	-	VDDI	V
9.	“L” Input Voltage	V_{IL}	-	V_{SS}	-	0.2VDDI	V
10.	“H” Output Voltage	V_{OH}	VDDI=2.7V, I_{OL}=1mA	0.8VDDI	-	VDDI	V
11.	“L” Output Voltage	V_{OL}	VDDI=2.7V, I_{OL}=1mA	V_{SS}	-	0.2VDDI	V
12.	Current Supply	I_{DD}	-	-	-	-	A

5.1 Backlight Options

NO	COLOR	FORWARD VOLTAGE (V)			FORWARD CURRENT (mA)			TYPICAL BRIGHTNESS (cd/m2) *
		Min	Typ.	Max	Min	Typ.	Max	
1.	White	-	3.3	-	-	180	240	3000

*Note : 1. Brightness measured at backlight surface.
2. On LCD surface, brightness is only about 10% to 15% of backlight brightness.
3. Lifetime of backlight: For YG, Amber, Red = 50K hrs. For White, Blue = 10K hrs

6.0 Environmental requirements

No	Test Item	Testing Condition	Remarks
1	High Temperature Operating	Ta = 70±5ºC 240h	
	Low temperature Operating	Ta = -20±5ºC 240h	
3	High Temperature, High Humidity Storage	Ta = 60±5ºC, RH=90%, 240h	
4	High Temperature Storage	Ta = 80±5ºC 240h	
5	Low temperature Storage	Ta = -30±5ºC 240h	
6	Thermal Shock	Ta = -20±5ºC ~ 70±5ºC, 10 min 10 min - 50cycle	

*Note: The background color and contrast ratio of LCD will vary throughout operating temperature range.

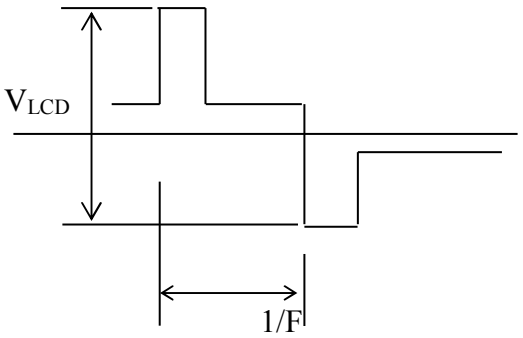
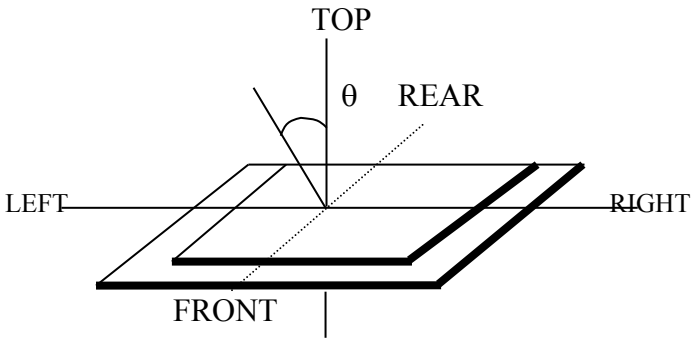
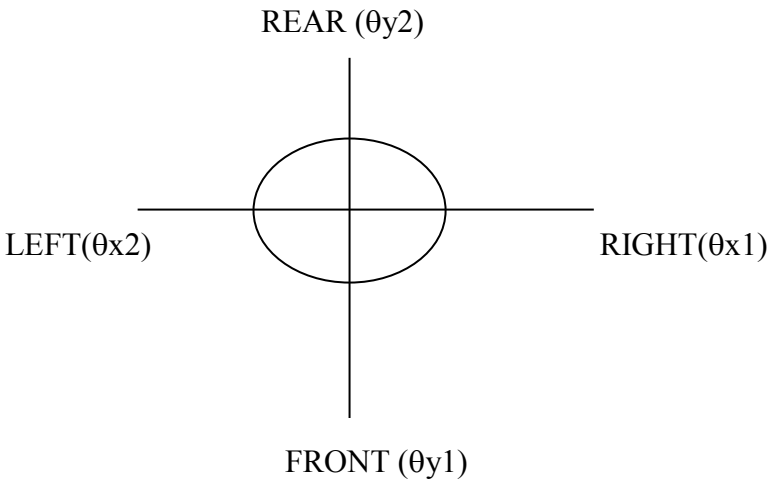
7.0 LCD specification

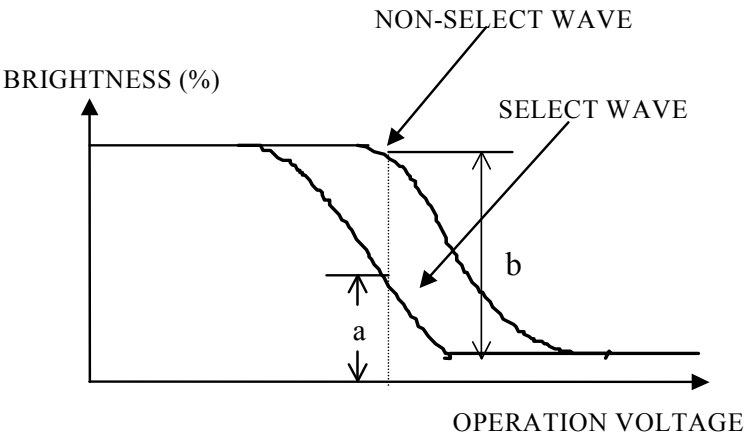
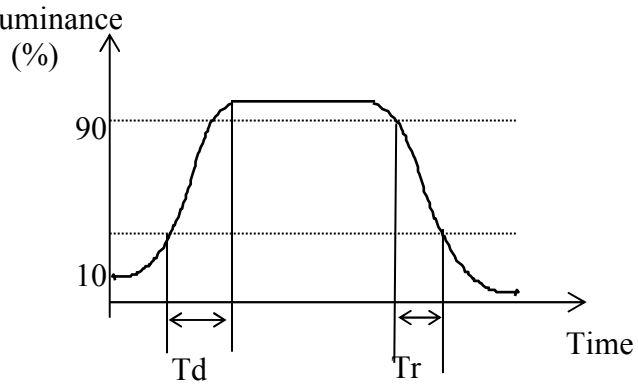
7.1 Electro-optical characteristics (at ambient temperature = 25°C)

NO	ITEM	SYMBOL	CONDITION	LCD TYPE UNIT	REF.
1.	Viewing Angle (Deg)	θ x 1	CR ≥ 250	50	7.1.2
		θ x 2		65	
		θ y 1		65	
		θ y 2		65	
2.	Contrast Ratio	CR	$\theta = 0^0$	800	7.1.3
3.	Response Time (msec)	Rise Time (Tr) + Decay Time (Td)	$\theta = 0^0$	35	7.1.4

*Note:

1. Viewing angle data is based on bottom view product by default. Should it be a top view product, values are then swap.
2. Contrast ratio is based on typical data when using white colour as backlight.
3. Equipment Used Eldim; Ez Contrast 120R , Spot Size = 2mm

NO	CHARACTERISTICS	DEFINITIONS
7.1.1	***Definition of Operating Voltage (V_{LCD})***	 V_{LCD} : Operating Voltage F : Frame Frequency
7.1.2	***Definition of Viewing Angle***	 

7.1.3	***Definition of Contrast Ratio***	 Contrast Ratio = Brightness of non-selected state (b) / Brightness of selected state (a) ***Conditions*** (a) Operating Voltage: V_{LCD} (b) Temperature: 25°C (c) Viewing Angle, θ = 0°
7.1.4	***Response Time***	 Tr: Measured between 10% and 90% of LCD segment maximum response with $V_{ON.}$ Td: With voltage switches to zero and the instant LCD segment reaches 10% of its maximum response.

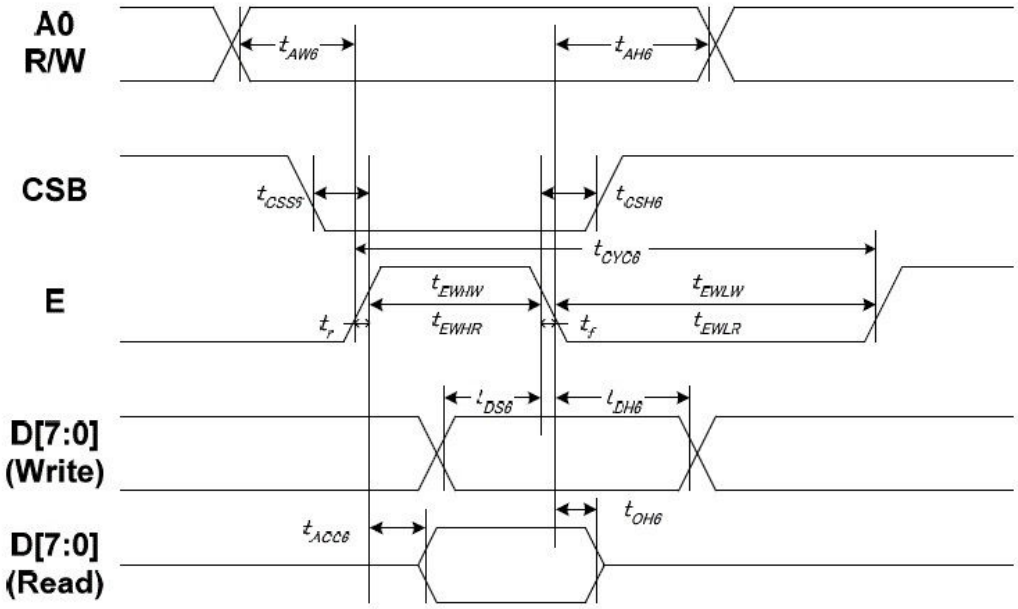
8.0 Interface

<table>
<tr><td>8.1</td><td>Display Driver</td><td colspan="2">ST7513 or equivalent</td></tr>
<tr><td>8.2</td><td>Pin No</td><td>Symbol</td><td>Description</td></tr>
<tr><td></td><td>1</td><td>GND</td><td>Ground</td></tr>
<tr><td></td><td>2</td><td>VDDA</td><td>Power supply for analog and booster circuit</td></tr>
<tr><td></td><td>3</td><td>VDDI</td><td>Power supply for IO system</td></tr>
<tr><td></td><td>4</td><td>D7 / SCL</td><td>8 bits bi-directional data bus / Serial input clock</td></tr>
<tr><td></td><td>5</td><td>D6</td><td>8 bits bi-directional data bus</td></tr>
<tr><td></td><td>6</td><td>D5</td><td>8 bits bi-directional data bus</td></tr>
<tr><td></td><td>7</td><td>D4</td><td>8 bits bi-directional data bus</td></tr>
<tr><td></td><td>8</td><td>D3</td><td>8 bits bi-directional data bus</td></tr>
<tr><td></td><td>9</td><td>D2</td><td>8 bits bi-directional data bus</td></tr>
<tr><td></td><td>10</td><td>D1</td><td>8 bits bi-directional data bus</td></tr>
<tr><td></td><td>11</td><td>D0 / SDA</td><td>8 bits bi-directional data bus / Serial data</td></tr>
<tr><td></td><td>12</td><td>A0</td><td>Register select input, H : Data / Parameter, L : Command</td></tr>
<tr><td></td><td>13</td><td>ERD</td><td>E : 6800 Series Parallel Interface Read & Write Control Input
/RD : 8080 Series Parallel Interface Read Enable Clock Input</td></tr>
<tr><td></td><td>14</td><td>RWR</td><td>R/W : 6800 Series Parallel Interface Read & Write Control Input
/WR : 8080 Series Parallel Interface Write Enable Clock Input</td></tr>
<tr><td></td><td>15</td><td>CSB</td><td>Chip select input, active low</td></tr>
<tr><td></td><td>16</td><td>RSTB</td><td>Reset input, active low</td></tr>
<tr><td></td><td>17</td><td>IF1</td><td rowspan="2">Select the interface mode
<table>
<tr><th>IF1</th><th>IF0</th><th>Selected Interface</th></tr>
<tr><td>L</td><td>L</td><td>8-bit 8080 parallel</td></tr>
<tr><td>L</td><td>H</td><td>8-bit 6800 parallel</td></tr>
<tr><td>H</td><td>L</td><td>3-line serial</td></tr>
<tr><td>H</td><td>H</td><td>4-line serial</td></tr>
</table></td></tr>
<tr><td></td><td>18</td><td>IF0</td></tr>
<tr><td></td><td>19</td><td>PX2SET</td><td>AVDD pump multiplier
<table>
<tr><th>PX2SET</th><th>AVDD pump multiplier</th><th>Description</th></tr>
<tr><td>H</td><td>x 2</td><td>VDDA = 5.0V</td></tr>
<tr><td>L</td><td>x 3</td><td>VDDA = 3.3V</td></tr>
</table></td></tr>
<tr><td></td><td>20</td><td>GND</td><td>Ground</td></tr>
<tr><td></td><td>21</td><td>A</td><td>LED anode</td></tr>
<tr><td></td><td>22</td><td>K</td><td>LED cathode</td></tr>
</table>

9.0 Functional Descriptions

9.1 Read/Write timing characteristics

System Bus Timing for 6800 Series MPU



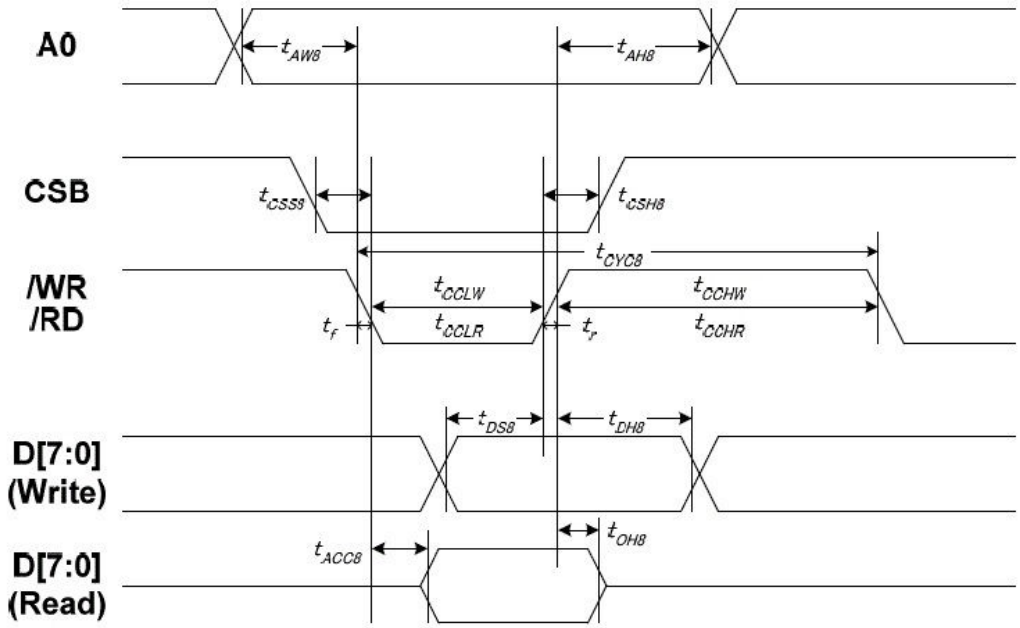
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		200	—	
Enable L pulse width (WRITE)		tEWLW		100	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
Enable L pulse width (READ)		tEWLR		130	—	
Enable H pulse width (READ)		tEWHR		130	—	
CSB setup time	CSB	tCSS6		100	—	
CSB hold time		tCSH6		100	—	
Write data setup time	D[7:0]	tDS6		70	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 100 pF	—	80	
Read data output disable time		tOH6	CL = 100 pF	15	80	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

System Bus Timing for 8080 Series MPU



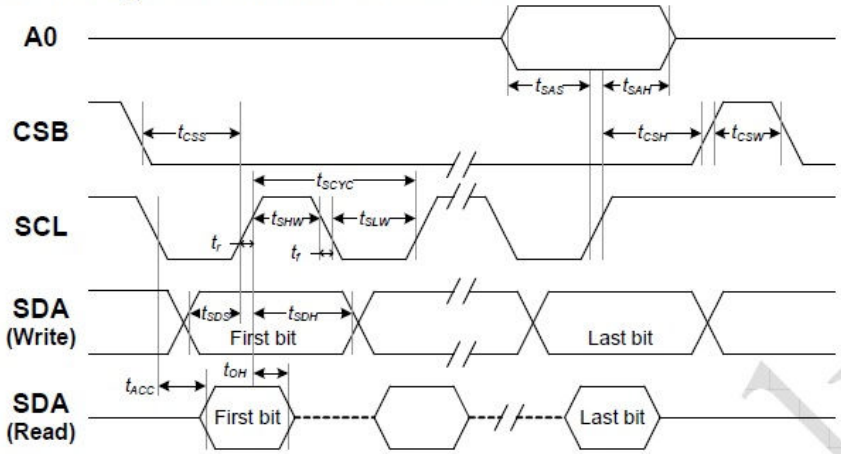
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		200	—	
/WR L pulse width (WRITE)		tCCLW		100	—	
/WR H pulse width (WRITE)		tCCHW		100	—	
/RD L pulse width (READ)	/RD	tCCLR		120	—	
/RD H pulse width (READ)		tCCHR		120	—	
CSB setup time	CSB	tCSS8		100	—	
CSB hold time		tCSH8		100	—	
WRITE Data setup time	D[7:0]	tDS8		70	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 100 pF	—	80	
READ Output disable time		tOH8	CL = 100 pF	15	80	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

System Bus Timing for 4-Line Serial Interface



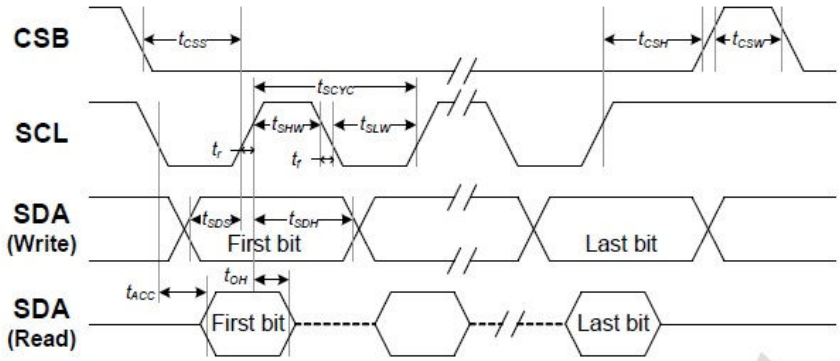
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = -40 ~ 105℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tSAS		32	—	ns
Address hold time		tSAH		28	—	
Serial clock period (Write)	SCL	tSCYC		60	—	
Serial clock period (Read)				110		
SCL “H” pulse width (Write)		tSHW		28	—	
SCL “H” pulse width (Read)				40		
SCL “L” pulse width (Write)		tSLW		32	—	
SCL “L” pulse width (Read)				70		
Write data setup time	SDA (Write)	tSDS		15	—	
Write data hold time		tSDH		20	—	
Read data access time	SDA (Read)	tACC		—	80	
Read data output disable time		tOH		15	80	
CSB-SCL time	CSB	tCSS		32	—	
CSB-SCL time		tCSH		28	—	
CSB “H” pulse width		tCSW		15	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

System Bus Timing for 3-Line Serial Interface



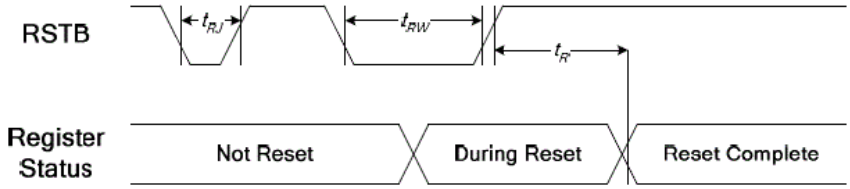
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, -40 ~ 105℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period (Write)	SCL	tSCYC		60	—	ns
Serial clock period (Read)				110	—	
SCL "H" pulse width (Write)		tSHW		28	—	
SCL "H" pulse width (Read)				40	—	
SCL "L" pulse width (Write)		tSLW		32	—	
SCL "L" pulse width (Read)				70	—	
Write data setup time	SDA (Write)	tSDS		15	—	
Write data hold time		tSDH		20	—	
Read data access time	SDA (Read)	tACC		—	80	
Read data output disable time		tOH		15	80	
CSB-SCL time	CSB	tCSS		28	—	
CSB-SCL time		tCSH		32	—	
CSB "H" pulse width		tCSW		15	—	

Note:

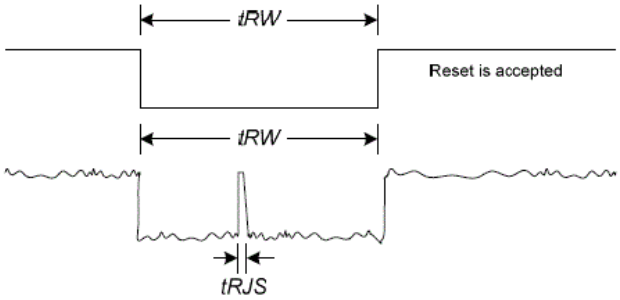
1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

Hardware Reset Timing



AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 *1	us
Reset "L" pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns

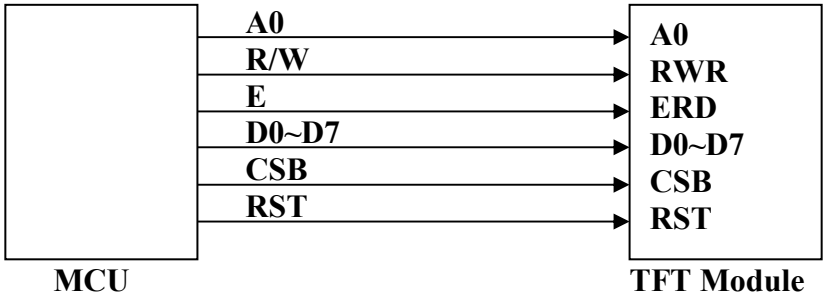


Note:

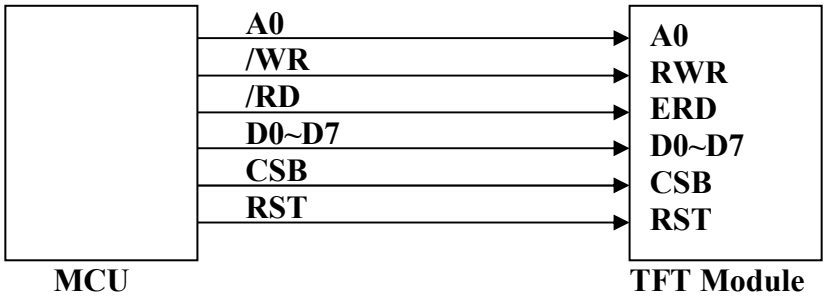
1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than tRW specified above. If the LOW pulse is less than tRJ specified above, the reset procedure of IC will not start. If the LOW pulse is longer than tRJ and less than tRW, the reset procedure of IC is not guaranteed.

9.2 Application Circuits

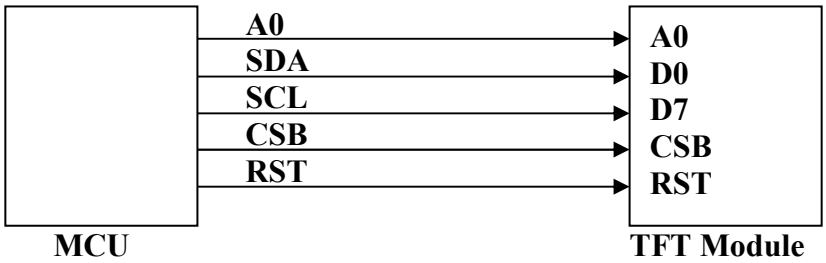
9.2.1 6800 – Series Parallel Interface



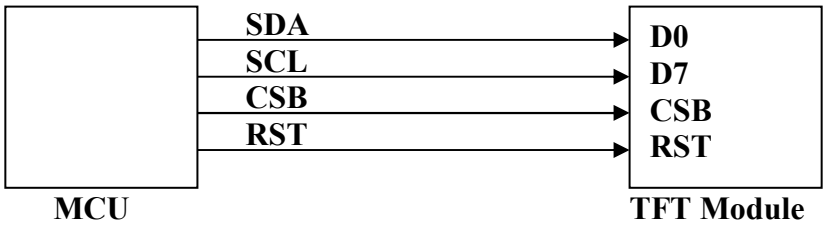
9.2.2 8080 – Series Parallel Interface



9.2.3 4-line Serial Interface



9.2.4 3-line Serial Interface



10.0 Instruction set

Instruction	Add. (hex)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	↑	0	0	0	0	0	0	0	0		Non-Operation
		1	1	↑	1	0	1	0	0	1	0	1		
SLPOUT	12	0	1	↑	0	0	0	1	0	0	1	0		Sleep Out
		1	1	↑	1	0	1	0	0	1	0	1		
SLPIN	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep In
		1	1	↑	1	0	1	0	0	1	0	1		
DISOFF	14	0	1	↑	0	0	0	1	0	1	0	0		Display Off
		1	1	↑	1	0	1	0	0	1	0	1		
DISON	15	0	1	↑	0	0	0	1	0	1	0	1		Display On
		1	1	↑	1	0	1	0	0	1	0	1		
DINVOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Display Invert Out
		1	1	↑	1	0	1	0	0	1	0	1		
DINVIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Display Invert In
		1	1	↑	1	0	1	0	0	1	0	1		
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out
		1	1	↑	1	0	1	0	0	1	0	1		
BLIN	1D	0	1	↑	0	0	0	1	1	1	0	1		Blinking In
		1	1	↑	1	0	1	0	0	1	0	1		
STFRAME	21	0	1	↑	0	0	1	0	0	0	0	1		Start Frame Address
		1	1	↑	0	0	0	0	0	0	SFrmA1	SFrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	22	0	1	↑	0	0	1	0	0	0	1	0		BPP Select
		1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MADCTL	24	0	1	↑	0	0	1	0	0	1	0	0		Memory Address Control
		1	1	↑	0	0	0	0	0	MV	MY	MX	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PASET	25	0	1	↑	0	0	1	0	0	1	0	1		Page Address Set
		1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00	
		1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	77	
		1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
CASET	26	0	1	↑	0	0	1	0	0	1	1	0		Column

		1	1	↑	0	0	0	0	0	0	0	CSA8	00	Address Set
		1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00	
		1	1	↑	0	0	0	0	0	0	0	CEA8	01	
		1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	8F	
BLKFIL	29	0	1	↑	0	0	1	0	1	0	0	1		Block Fill
		1	1	↑	0	0	0	0	BFData3	BFData2	BFData1	BFData0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BLSET	2B	0	1	↑	0	0	1	0	1	0	1	1		Blinking Set
		1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D	
		1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
WRRAM	2C	0	1	↑	0	0	1	0	1	1	0	0		Write RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
RDRAM	2D	0	1	↑	0	0	1	0	1	1	0	1		Read RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	X	X	X	X	X	X	X	X		
		1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
DISAR	31	0	1	↑	0	0	1	1	0	0	0	1		Display Area
		1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	EF	
		1	1	↑	0	0	0	0	0	0	0	1	01	
		1	1	↑	1	0	0	0	1	1	1	1	8F	
		1	1	↑	1	0	1	0	0	1	0	1		
DISSET1	32	0	1	↑	0	0	1	1	0	0	1	0		Display Set1
		1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	43	
		1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	02	
		1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00	
		1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01	
DISSET2	33	0	1	↑	0	0	1	1	0	0	1	1		Display Set2
		1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A	
		1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	3A	
		1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C	
		1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	38	
PTLSET1	34	0	1	↑	0	0	1	1	0	1	0	0		Partial Set 1
		1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00	
		1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PTLSET2	35	0	1	↑	0	0	1	1	0	1	0	1		Partial Set 2
		1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00	
		1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	00	
		1	1	↑	1	0	1	0	0	1	0	1		

		1	1	↑	1	0	1	0	0	1	0	1		
PTLSET3	36	0	1	↑	0	0	1	1	0	1	1	0		Partial Set 3
		1	1	↑	0	NDisRefR6	NDisRefR5	NDisRefR4	NDisRefR3	NDisRefR2	NDisRefR1	NDisRefR0	00	
		1	1	↑	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0	00	
		1	1	↑	0	0	0	0	0	0	NDisDM1	NDisDM0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
VCMDAT	54	0	1	↑	0	1	0	1	0	1	0	0		VCOM Offset Data
		1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00	
		1	1	↑	VcomD17	VcomD16	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00	
		1	1	↑	VcomD17	VcomD26	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00	
		1	1	↑	1	0	1	0	0	1	0	1		
UIDSET	55	0	1	↑	0	1	0	1	0	1	0	1		User ID
		1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00	
		1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MTPMOD	5A	0	1	↑	0	1	0	1	1	0	1	0		Multi Time PROM Mode
		1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MTPOP	5B	0	1	↑	0	1	0	1	1	0	1	1		Multi Time PROM Operation
		1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
SPI3WRCNT	5C	0	1	↑	0	1	0	1	1	1	0	0		SPI3 Write Memory Byte Counter
		1	1	↑	Si3Mw15	Si3Mw14	Si3Mw13	Si3Mw12	Si3Mw11	Si3Mw10	Si3Mw9	Si3Mw8	01	
		1	1	↑	Si3Mw7	Si3Mw6	Si3Mw5	5Si3Mw4	Si3Mw3	Si3Mw2	Si3Mw1	Si3Mw0	8F	
		1	1	↑										
		1	1	↑										
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control
		1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40	
		1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	04	
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET1	62	0	1	↑	0	1	1	0	0	0	1	0		Electronic Volume Set 1
		1	1	↑	VCOM7	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A	
		1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06	
		1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET2	63	0	1	↑	0	1	1	0	0	0	1	1		Electronic Volume Set 2
		1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F	
		1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		

		1	1	↑	1	0	1	0	0	1	0	1		
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting
		1	1	↑	0	AVclClk2	AVclClk1	AVclClk0	0	AVdClk2	AVdClk2	AVdClk2	44	
		1	1	↑	0	VglClk2	VglClk1	VglClk0	0	Vghclk2	Vghclk1	VghClk0	44	
		1	1	↑	0	AVclClk_nd2	AVclClk_nd1	AVclClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44	
		1	1	↑	0	VglClk_nd2	VglClk_nd1	VglClk_nd0	0	Vghclk_nd2	Vghclk_nd1	VghClk_nd0	44	
GATESET	66	0	1	↑	0	1	1	0	0	1	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWMCTRL	6C	0	1	↑	0	1	1	0	1	1	0	0		PWM Control
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00	
		1	1	↑	SLEDOn7	SLEDOn6	SLEDOn5	SLEDOn4	SLEDOn3	SLEDOn2	SLEDOn1	SLEDOn0		
		1	1	↑	ASLEDOn7	ASLEDOn6	ASLEDOn5	ASLEDOn4	ASLEDOn3	ASLEDOn2	ASLEDOn1	ASLEDOn0		
		1	1	↑	ASLEDOf7	ASLEDOf6	ASLEDOf5	ASLEDOf4	ASLEDOf3	ASLEDOf2	ASLEDOf1	ASLEDOf0		
RDSTAT	72	0	1	↑	0	1	1	1	0	0	1	0		Read Status
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	0	R13	R12	R11	R10		
		1	↑	1	0	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
RDREV	73	0	1	↑	0	1	1	1	0	0	1	1		Read Revision
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
RDUID	75	0	1	↑	0	1	1	1	0	1	0	1		Read User ID
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
RDVCMDAT	79	0	1	↑	0	1	1	1	1	0	0	1		Read VCOM Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50		
		1	↑	1	x	x	x	x	R63	R62	R61	R60		
GAMSET4P1	91	0	1	↑	1	0	0	1	0	0	0	1		Gamma Set 4bpp Positive 1
		1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00	
		1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04	
		1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08	
		1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C	
GAMSET4P2	92	0	1	↑	1	0	0	1	0	0	1	0		Gamma Set

		1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10	4bpp Positive
		1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14	2
		1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18	
		1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C	
GAMSET4P3	93	0	1	↑	1	0	0	1	0	0	1	1		
		1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23	Gamma Set
		1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27	4bpp Positive
		1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B	3
		1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F	
GAMSET4P4	94	0	1	↑	1	0	0	1	0	1	0	0		
		1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33	Gamma Set
		1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37	4bpp Positive
		1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B	4
		1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F	
GAMSET2P	95	0	1	↑	1	0	0	1	0	1	0	1		
		1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00	Gamma Set
		1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15	2bpp Positive
		1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A	
		1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F	
GAMSET1	96	0	1	↑	1	0	0	1	0	1	1	0		
		1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00	Gamma Set
		1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F	1bpp
		1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00	
		1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F	
GAMSET4N1	99	0	1	↑	1	0	0	1	1	0	0	1		
		1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00	Gamma Set
		1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04	4bpp
		1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08	Negative 1
		1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	0C	
GAMSET4N2	9A	0	1	↑	1	0	0	1	1	0	1	0		
		1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10	Gamma Set
		1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14	4bpp
		1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18	Negative 2
		1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C	
GAMSET4N3	9B	0	1	↑	1	0	0	1	1	0	1	1		
		1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23	Gamma Set
		1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27	4bpp
		1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B	Negative 3
		1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
GAMSET4N4	9C	0	1	↑	1	0	0	1	1	1	0	0		
		1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	Gamma Set
		1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37	4bpp
		1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	Negative 4
		1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F	
GAMSET2N	9D	0	1	↑	1	0	0	1	1	1	0	1		Gamma Set

		1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	2bpp
		1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	Negative
		1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
		1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F	
RMWIN	A1	0	1	↑	1	0	1	0	0	0	0	1		Read Modify
		1	1	↑	1	0	1	0	0	1	0	1		Write In
MTPRDEN	A2	0	1	↑	1	0	1	0	0	0	1	0		MTP Read
		1	1	↑	1	0	1	0	0	1	0	1		Enable
MTPWREN	A3	0	1	↑	1	0	1	0	0	0	1	1		MTP Write
		1	1	↑	1	0	1	0	0	1	0	1		Enable
PTLOUT	A9	0	1	↑	1	0	1	0	1	0	0	1		Partial Out
		1	1	↑	1	0	1	0	0	1	0	1		
PTLIN	AA	0	1	↑	1	0	1	0	1	0	1	0		Partial In
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify
		1	1	↑	1	0	1	0	0	1	0	1		Write Out
SWRESET	AE	0	1	↑	1	0	1	0	1	1	1	0		Software
		1	1	↑	1	0	1	0	0	1	0	1		Reset
RDTC	76	0	1	↑	0	1	1	1	0	1	1	0		Read TC Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	0	0	0	0	0	0	0	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
TCVCOM	B1	0	1	↑	1	0	1	1	0	0	0	1		TCVCOM
		1	1	↑	0	0	0	TCAVCM4	TCAVCM3	TCAVCM2	TCAVCM1	TCAVCM0	00	Offset Set
		1	1	↑	0	0	0	TCBVCM4	TCBVCM3	TCBVCM2	TCBVCM1	TCBVCM0	00	
		1	1	↑	0	0	0	TCCVCM4	TCCVCM3	TCCVCM2	TCCVCM1	TCCVCM0	00	
		1	1	↑	0	0	0	TCDVCM4	TCDVCM3	TCDVCM2	TCDVCM1	TCDVCM0	00	
TCPWMSY	B2	0	1	↑	1	0	1	1	0	0	1	0		TC PWM Sync
		1	1	↑	TCAPS7	TCAPS6	TCAPS5	TCAPS4	TCAPS3	TCAPS2	TCAPS1	TCAPS0	00	Offset Set
		1	1	↑	TCBPS7	TCBPS6	TCBPS5	TCBPS4	TCBPS3	TCBPS2	TCBPS1	TCBPS0	00	
		1	1	↑	TCCPS7	TCCPS6	TCCPS5	TCCPS4	TCCPS3	TCCPS2	TCCPS1	TCCPS0	00	
		1	1	↑	TCDPS7	TCDPS6	TCDPS5	TCDPS4	TCDPS3	TCDPS2	TCDPS1	TCDPS0	00	
TCPWMASON	B3	0	1	↑	1	0	1	1	0	0	1	1		
		1	1	↑	TCAPAsOn7	TCAPAsOn6	TCAPAsOn5	TCAPAsOn4	TCAPAsOn3	TCAPAsOn2	TCAPAsOn1	TCAPAsOn0	00	
		1	1	↑	TCBPAsOn7	TCBPAsOn6	TCBPAsOn5	TCBPAsOn4	TCBPAsOn3	TCBPAsOn2	TCBPAsOn1	TCBPAsOn0	00	
		1	1	↑	TCCPAsOn7	TCCPAsOn6	TCCPAsOn5	TCCPAsOn4	TCCPAsOn3	TCCPAsOn2	TCCPAsOn1	TCCPAsOn0	00	
		1	1	↑	TCDPAsOn7	TCDPAsOn6	TCDPAsOn5	TCDPAsOn4	TCDPAsOn3	TCDPAsOn2	TCDPAsOn1	TCDPAsOn0	00	
TCPWMASOF	B4	0	1	↑	1	0	1	1	0	1	0	0		
		1	1	↑	TCAPAsOf7	TCAPAsOf6	TCAPAsOf5	TCAPAsOf4	TCAPAsOf3	TCAPAsOf2	TCAPAsOf1	TCAPAsOf0	00	
		1	1	↑	TCBPAsOf7	TCBPAsOf6	TCBPAsOf5	TCBPAsOf4	TCBPAsOf3	TCBPAsOf2	TCBPAsOf1	TCBPAsOf0	00	
		1	1	↑	TCCPAsOf7	TCCPAsOf6	TCCPAsOf5	TCCPAsOf4	TCCPAsOf3	TCCPAsOf2	TCCPAsOf1	TCCPAsOf0	00	
		1	1	↑	TCDPAsOf7	TCDPAsOf6	TCDPAsOf5	TCDPAsOf4	TCDPAsOf3	TCDPAsOf2	TCDPAsOf1	TCDPAsOf0	00	
TCVGH1	B5	0	1	↑	1	0	1	1	0	1	0	1		TC VGHREG
		1	1	↑	0	TCAVGH6	TCAVGH5	TCAVGH4	TCAVGH3	TCAVGH2	TCAVGH1	TCAVGH0	00	Offset Set
		1	1	↑	0	TCBVGH6	TCBVGH5	TCBVGH4	TCBVGH3	TCBVGH2	TCBVGH1	TCBVGH0	00	

		1	1	↑	0	TCCVGH6	TCCVGH5	TCCVGH4	TCCVGH3	TCCVGH2	TCCVGH1	TCCVGH0	00	
		1	1	↑	0	TCDVGH6	TCDVGH5	TCDVGH4	TCDVGH3	TCDVGH2	TCDVGH1	TCDVGH0	00	
TCVGH2	B6	0	1	↑	1	0	1	1	0	1	1	0		TC VGLREG Offset Set
		1	1	↑	TCAGIx1	TCAGIx0	TCAVGL5	TCAVGL4	TCAVGL3	TCAVGL2	TCAVGL1	TCAVGL0	00	
		1	1	↑	TCBGIx1	TCBGIx0	TCBVGL5	TCBVGL4	TCBVGL3	TCBVGL2	TCBVGL1	TCBVGL0	00	
		1	1	↑	TCCGIx1	TCCGIx0	TCCVGL5	TCCVGL4	TCCVGL3	TCCVGL2	TCCVGL1	TCCVGL0	00	
		1	1	↑	TCDGIx1	TCDGIx0	TCDVGL5	TCDVGL4	TCDVGL3	TCDVGL2	TCDVGL1	TCDVGL0	00	
SETTCGVD1	C1	0	1	↑	1	1	0	0	0	0	0	1		Set GVDD TC Gradient Curves1
		1	1	↑	MTGVD13	MTGVD12	MTGVD11	MTGVD10	MTGVD03	MTGVD02	MTGVD01	MTGVD00	00	
		1	1	↑	MTGVD33	MTGVD32	MTGVD31	MTGVD30	MTGVD23	MTGVD22	MTGVD21	MTGVD20	00	
		1	1	↑	MTGVD53	MTGVD52	MTGVD51	MTGVD50	MTGVD43	MTGVD42	MTGVD41	MTGVD40	00	
		1	1	↑	MTGVD73	MTGVD72	MTGVD71	MTGVD70	MTGVD63	MTGVD62	MTGVD61	MTGVD60	00	
SETTCGVD2	C2	0	1	↑	1	1	0	0	0	0	1	0		Set GVDD TC Gradient Curves2
		1	1	↑	MTGVD93	MTGVD92	MTGVD91	MTGVD90	MTGVD83	MTGVD82	MTGVD81	MTGVD80	00	
		1	1	↑	MTGVDB3	MTGVDB2	MTGVDB1	MTGVDB0	MTGVDA3	MTGVDA2	MTGVDA1	MTGVDA0	00	
		1	1	↑	MTGVDD3	MTGVDD2	MTGVDD1	MTGVDD0	MTGVDC3	MTGVDC2	MTGVDC1	MTGVDC0	00	
		1	1	↑	MTGVDF3	MTGVDF2	MTGVDF1	MTGVDF0	MTGVDE3	MTGVDE2	MTGVDE1	MTGVDE0	00	
SETTCGVD3	C3	0	1	↑	1	1	0	0	0	0	1	1		Set GVDD TC Gradient Curves3
		1	1	↑	MTGVD113	MTGVD112	MTGVD111	MTGVD110	MTGVD103	MTGVD102	MTGVD101	MTGVD100	00	
		1	1	↑	0	0	THGVD5	THGVD4	THGVD3	THGVD2	THGVD1	THGVD0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
SETTCGVC1	C4	0	1	↑	1	1	0	0	0	1	0	0		Set GVCL TC Gradient Curves1
		1	1	↑	MTGVC13	MTGVC12	MTGVC11	MTGVC10	MTGVC03	MTGVC02	MTGVC01	MTGVC00	00	
		1	1	↑	MTGVC33	MTGVC32	MTGVC31	MTGVC30	MTGVC23	MTGVC22	MTGVC21	MTGVC20	00	
		1	1	↑	MTGVC53	MTGVC52	MTGVC51	MTGVC50	MTGVC43	MTGVC42	MTGVC41	MTGVC40	00	
		1	1	↑	MTGVC73	MTGVC72	MTGVC71	MTGVC70	MTGVC63	MTGVC62	MTGVC61	MTGVC60	00	
SETTCGVC2	C5	0	1	↑	1	1	0	0	0	1	0	1		Set GVCL TC Gradient Curves2
		1	1	↑	MTGVC93	MTGVC92	MTGVC91	MTGVC90	MTGVC83	MTGVC82	MTGVC81	MTGVC80	00	
		1	1	↑	MTGVCB3	MTGVCB2	MTGVCB1	MTGVCB0	MTGVCA3	MTGVCA2	MTGVCA1	MTGVCA0	00	
		1	1	↑	MTGVCD3	MTGVCD2	MTGVCD1	MTGVCD0	MTGVCC3	MTGVCC2	MTGVCC1	MTGVCC0	00	
		1	1	↑	MTGVCF3	MTGVCF2	MTGVCF1	MTGVCF0	MTGVCE3	MTGVCE2	MTGVCE1	MTGVCE0	00	
SETTCGVC3	C6	0	1	↑	1	1	0	0	0	1	1	0		Set GVCL TC Gradient Curves3
		1	1	↑	MTGVC113	MTGVC112	MTGVC111	MTGVC110	MTGVC103	MTGVC102	MTGVC101	MTGVC100	00	
		1	1	↑	0	0	THGVC5	THGVC4	THGVC3	THGVC2	THGVC1	THGVC0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
SETTCVGH	C7	0	1	↑	1	1	0	0	0	1	1	1		Set TC VGH Flag
		1	1	↑	TAVGH7	TAVGH6	TAVGH5	TAVGH4	TAVGH3	TAVGH2	TAVGH1	TAVGH0	00	
		1	1	↑	TBVGH7	TBVGH6	TBVGH5	TBVGH4	TBVGH3	TBVGH2	TBVGH1	TBVGH0	00	
		1	1	↑	TCVGH7	TCVGH6	TCVGH5	TCVGH4	TCVGH3	TCVGH2	TCVGH1	TCVGH0	00	
		1	1	↑	0	0	0	0	THVGH3	THVGH2	THVGH1	THVGH0	00	
SETTCVCOM	C8	0	1	↑	1	1	0	0	1	0	0	0		Set TC VCOM Flag
		1	1	↑	0	TAVCOM6	TAVCOM5	TAVCOM4	TAVCOM3	TAVCOM2	TAVCOM1	TAVCOM0	00	
		1	1	↑	0	TBVCOM6	TBVCOM5	TBVCOM4	TBVCOM3	TBVCOM2	TBVCOM1	TBVCOM0	00	

		1	1	↑	0	TCVCOM6	TCVCOM5	TCVCOM4	TCVCOM3	TCVCOM2	TCVCOM1	TCVCOM0	00	
		1	1	↑	0	0	0	0	THVCOM3	THVCOM2	THVCOM1	THVCOM0	00	
SETTCFRM	C9	0	1	↑	1	1	0	0	1	0	0	1		Set TC FRC Flag
		1	1	↑	0	TAFRM6	TAFRM5	TAFRM4	TAFRM3	TAFRM2	TAFRM1	TAFRM0	00	
		1	1	↑	0	TBFRM6	TBFRM5	TBFRM4	TBFRM3	TBFRM2	TBFRM1	TBFRM0	00	
		1	1	↑	0	TCFRM6	TCFRM5	TCFRM4	TCFRM3	TCFRM2	TCFRM1	TCFRM0	00	
		1	1	↑	0	0	0	0	THFRM3	THFRM2	THFRM1	THFRM0	00	
SETTCGMA	CA	0	1	↑	1	1	0	0	1	0	1	0		Set TC Gamma Flag
		1	1	↑	0	TAGMA6	TAGMA5	TAGMA4	TAGMA3	TAGMA2	TAGMA1	TAGMA0	00	
		1	1	↑	0	TBGMA6	TBGMA5	TBGMA4	TBGMA3	TBGMA2	TBGMA1	TBGMA0	00	
		1	1	↑	0	TCGMA6	TCGMA5	TCGMA4	TCGMA3	TCGMA2	TCGMA1	TCGMA0	00	
		1	1	↑	0	0	0	0	THGMA3	THGMA2	THGMA1	THGMA0	00	
SETTCPWM	CB	0	1	↑	1	1	0	0	1	0	1	1		Set TC PWM Flag
		1	1	↑	0	TAPWM6	TAPWM5	TAPWM4	TAPWM3	TAPWM2	TAPWM1	TAPWM0	00	
		1	1	↑	0	TBPWM6	TBPWM5	TBPWM4	TBPWM3	TBPWM2	TBPWM1	TBPWM0	00	
		1	1	↑	0	TCPWM6	TCPWM5	TCPWM4	TCPWM3	TCPWM2	TCPWM1	TCPWM0	00	
		1	1	↑	0	0	0	0	THPWM3	THPWM2	THPWM1	THPWM0	00	
TCFP	CC	0	1	↑	1	1	0	0	1	1	0	0		Front Porch of Frame Rate TC Range Setting
		1	1	↑	TCAFP7	TCAFP6	TCAFP5	TCAFP4	TCAFP3	TCAFP2	TCAFP1	TCAFP0	00	
		1	1	↑	TCBFP7	TCBFP6	TCBFP5	TCBFP4	TCBFP3	TCBFP2	TCBFP1	TCBFP0	00	
		1	1	↑	TCCFP7	TCCFP6	TCCFP5	TCCFP4	TCCFP3	TCCFP2	TCCFP1	TCCFP0	00	
		1	1	↑	TCDFP7	TCDFP6	TCDFP5	TCDFP4	TCDFP3	TCDFP2	TCDFP1	TCDFP0	00	
TC1H	CD	0	1	↑	1	1	0	0	1	1	0	1		1H of Frame Rate TC Range Setting
		1	1	↑	TCAGLW7	TCAGLW6	TCAGLW5	TCAGLW4	TCAGLW3	TCAGLW2	TCAGLW1	TCAGLW0	00	
		1	1	↑	TCBGLW7	TCBGLW6	TCBGLW5	TCBGLW4	TCBGLW3	TCBGLW2	TCBGLW1	TCBGLW0	00	
		1	1	↑	TCCGLW7	TCCGLW6	TCCGLW5	TCCGLW4	TCCGLW3	TCCGLW2	TCCGLW1	TCCGLW0	00	
		1	1	↑	TCDGLW7	TCDGLW6	TCDGLW5	TCDGLW4	TCDGLW3	TCDGLW2	TCDGLW1	TCDGLW0	00	
TCBP	CE	0	1	↑	1	1	0	0	1	1	1	0		Back Porch of Frame Rate TC Range Setting
		1	1	↑	TCABP7	TCABP6	TCABP5	TCABP4	TCABP3	TCABP2	TCABP1	TCABP0	00	
		1	1	↑	TCBBP7	TCBBP6	TCBBP5	TCBBP4	TCBBP3	TCBBP2	TCBBP1	TCBBP0	00	
		1	1	↑	TCCBP7	TCCBP6	TCCBP5	TCCBP4	TCCBP3	TCCBP2	TCCBP1	TCCBP0	00	
		1	1	↑	F	TCDBP6	TCDBP5	TCDBP4	TCDBP3	TCDBP2	TCDBP1	TCDBP0	00	
TC4GPA1	D0	0	1	↑	1	1	0	1	0	0	0	0		Gamma 4BPP TC Range A Positive polarity
		1	1	↑	TCA4GP13	TCA4GP12	TCA4GP11	TCA4GP10	TCA4GP03	TCA4GP02	TCA4GP01	TCA4GP00	00	
		1	1	↑	TCA4GP33	TCA4GP32	TCA4GP31	TCA4GP30	TCA4GP23	TCA4GP22	TCA4GP21	TCA4GP20	00	
		1	1	↑	TCA4GP53	TCA4GP52	TCA4GP51	TCA4GP50	TCA4GP43	TCA4GP42	TCA4GP41	TCA4GP40	00	
		1	1	↑	TCA4GP73	TCA4GP72	TCA4GP71	TCA4GP70	TCA4GP63	TCA4GP62	TCA4GP61	TCA4GP60	00	
TC4GPA2	D1	0	1	↑	1	1	0	1	0	0	0	1		Gamma 4BPP TC Range A Positive polarity
		1	1	↑	TCA4GP93	TCA4GP92	TCA4GP91	TCA4GP90	TCA4GP83	TCA4GP82	TCA4GP81	TCA4GP80	00	
		1	1	↑	TCA4GPB3	TCA4GPB2	TCA4GPB1	TCA4GPB0	TCA4GPA3	TCA4GPA2	TCA4GPA1	TCA4GPA0	00	
		1	1	↑	TCA4GPD3	TCA4GPD2	TCA4GPD1	TCA4GPD0	TCA4GPC3	TCA4GPC2	TCA4GPC1	TCA4GPC0	00	
		1	1	↑	TCA4GPF3	TCA4GPF2	TCA4GPF1	TCA4GPF0	TCA4GPE3	TCA4GPE2	TCA4GPE1	TCA4GPE0	00	
TC4GNA1	D2	0	1	↑	1	1	0	1	0	0	1	0		Gamma 4BPP TC Range A Negative
		1	1	↑	TCA4GN13	TCA4GN12	TCA4GN11	TCA4GN10	TCA4GN03	TCA4GN02	TCA4GN01	TCA4GN00	00	
		1	1	↑	TCA4GN33	TCA4GN32	TCA4GN31	TCA4GN30	TCA4GN23	TCA4GN22	TCA4GN21	TCA4GN20	00	

		1	1	↑	TCA4GN53	TCA4GN52	TCA4GN51	TCA4GN50	TCA4GN43	TCA4GN42	TCA4GN41	TCA4GN40	00	polarity
		1	1	↑	TCA4GN73	TCA4GN72	TCA4GN71	TCA4GN70	TCA4GN63	TCA4GN62	TCA4GN61	TCA4GN60	00	
TC4GNA2	D3	0	1	↑	1	1	0	1	0	0	1	1		Gamma 4BPP TC Range A Negative polarity
		1	1	↑	TCA4GN93	TCA4GN92	TCA4GN91	TCA4GN90	TCA4GN83	TCA4GN82	TCA4GN81	TCA4GN80	00	
		1	1	↑	TCA4GNB3	TCA4GNB2	TCA4GNB1	TCA4GNB0	TCA4GNA3	TCA4GNA2	TCA4GNA1	TCA4GNA0	00	
		1	1	↑	TCA4GND3	TCA4GND2	TCA4GND1	TCA4GND0	TCA4GNC3	TCA4GNC2	TCA4GNC1	TCA4GNC0	00	
		1	1	↑	TCA4GNF3	TCA4GNF2	TCA4GNF1	TCA4GNF0	TCA4GNE3	TCA4GNE2	TCA4GNE1	TCA4GNE0	00	
TC4GPB1	D4	0	1	↑	1	1	0	1	0	1	0	0		Gamma 4BPP TC Range B Positive polarity
		1	1	↑	TCB4GP13	TCB4GP12	TCB4GP11	TCB4GP10	TCB4GP03	TCB4GP02	TCB4GP01	TCB4GP00	00	
		1	1	↑	TCB4GP33	TCB4GP32	TCB4GP31	TCB4GP30	TCB4GP23	TCB4GP22	TCB4GP21	TCB4GP20	00	
		1	1	↑	TCB4GP53	TCB4GP52	TCB4GP51	TCB4GP50	TCB4GP43	TCB4GP42	TCB4GP41	TCB4GP40	00	
		1	1	↑	TCB4GP73	TCB4GP72	TCB4GP71	TCB4GP70	TCB4GP63	TCB4GP62	TCB4GP61	TCB4GP60	00	
TC4GPB2	D5	0	1	↑	1	1	0	1	0	1	0	1		Gamma 4BPP TC Range B Positive polarity
		1	1	↑	TCB4GP93	TCB4GP92	TCB4GP91	TCB4GP90	TCB4GP83	TCB4GP82	TCB4GP81	TCB4GP80	00	
		1	1	↑	TCB4GPB3	TCB4GPB2	TCB4GPB1	TCB4GPB0	TCB4GPA3	TCB4GPA2	TCB4GPA1	TCB4GPA0	00	
		1	1	↑	TCB4GPD3	TCB4GPD2	TCB4GPD1	TCB4GPD0	TCB4GPC3	TCB4GPC2	TCB4GPC1	TCB4GPC0	00	
		1	1	↑	TCB4GPF3	TCB4GPF2	TCB4GPF1	TCB4GPF0	TCB4GPE3	TCB4GPE2	TCB4GPE1	TCB4GPE0	00	
TC4GNB1	D6	0	1	↑	1	1	0	1	0	1	1	0		Gamma 4BPP TC Range B Negative polarity
		1	1	↑	TCB4GN13	TCB4GN12	TCB4GN11	TCB4GN10	TCB4GN03	TCB4GN02	TCB4GN01	TCB4GN00	00	
		1	1	↑	TCB4GN33	TCB4GN32	TCB4GN31	TCB4GN30	TCB4GN23	TCB4GN22	TCB4GN21	TCB4GN20	00	
		1	1	↑	TCB4GN53	TCB4GN52	TCB4GN51	TCB4GN50	TCB4GN43	TCB4GN42	TCB4GN41	TCB4GN40	00	
		1	1	↑	TCB4GN73	TCB4GN72	TCB4GN71	TCB4GN70	TCB4GN63	TCB4GN62	TCB4GN61	TCB4GN60	00	
TC4GNB2	D7	0	1	↑	1	1	0	1	0	1	1	1		Gamma 4BPP TC Range B Negative polarity
		1	1	↑	TCB4GN93	TCB4GN92	TCB4GN91	TCB4GN90	TCB4GN83	TCB4GN82	TCB4GN81	TCB4GN80	00	
		1	1	↑	TCB4GNB3	TCB4GNB2	TCB4GNB1	TCB4GNB0	TCB4GNA3	TCB4GNA2	TCB4GNA1	TCB4GNA0	00	
		1	1	↑	TCB4GND3	TCB4GND2	TCB4GND1	TCB4GND0	TCB4GNC3	TCB4GNC2	TCB4GNC1	TCB4GNC0	00	
		1	1	↑	TCB4GNF3	TCB4GNF2	TCB4GNF1	TCB4GNF0	TCB4GNE3	TCB4GNE2	TCB4GNE1	TCB4GNE0	00	
TC4GPC1	D8	0	1	↑	1	1	0	1	1	0	0	0		Gamma 4BPP TC Range C Positive polarity
		1	1	↑	TCC4GP13	TCC4GP12	TCC4GP11	TCC4GP10	TCC4GP03	TCC4GP02	TCC4GP01	TCC4GP00	00	
		1	1	↑	TCC4GP33	TCC4GP32	TCC4GP31	TCC4GP30	TCC4GP23	TCC4GP22	TCC4GP21	TCC4GP20	00	
		1	1	↑	TCC4GP53	TCC4GP52	TCC4GP51	TCC4GP50	TCC4GP43	TCC4GP42	TCC4GP41	TCC4GP40	00	
		1	1	↑	TCC4GP73	TCC4GP72	TCC4GP71	TCC4GP70	TCC4GP63	TCC4GP62	TCC4GP61	TCC4GP60	00	
TC4GPC2	D9	0	1	↑	1	1	0	1	1	0	0	1		Gamma 4BPP TC Range C Positive polarity
		1	1	↑	TCC4GP93	TCC4GP92	TCC4GP91	TCC4GP90	TCC4GP83	TCC4GP82	TCC4GP81	TCC4GP80	00	
		1	1	↑	TCC4GPB3	TCC4GPB2	TCC4GPB1	TCC4GPB0	TCC4GPA3	TCC4GPA2	TCC4GPA1	TCC4GPA0	00	
		1	1	↑	TCC4GPD3	TCC4GPD2	TCC4GPD1	TCC4GPD0	TCC4GPC3	TCC4GPC2	TCC4GPC1	TCC4GPC0	00	
		1	1	↑	TCC4GPF3	TCC4GPF2	TCC4GPF1	TCC4GPF0	TCC4GPE3	TCC4GPE2	TCC4GPE1	TCC4GPE0	00	
TC4GNC1	DA	0	1	↑	1	1	0	1	1	0	1	0		Gamma 4BPP TC Range C Negative polarity
		1	1	↑	TCC4GN13	TCC4GN12	TCC4GN11	TCC4GN10	TCC4GN03	TCC4GN02	TCC4GN01	TCC4GN00	00	
		1	1	↑	TCC4GN33	TCC4GN32	TCC4GN31	TCC4GN30	TCC4GN23	TCC4GN22	TCC4GN21	TCC4GN20	00	
		1	1	↑	TCC4GN53	TCC4GN52	TCC4GN51	TCC4GN50	TCC4GN43	TCC4GN42	TCC4GN41	TCC4GN40	00	
		1	1	↑	TCC4GN73	TCC4GN72	TCC4GN71	TCC4GN70	TCC4GN63	TCC4GN62	TCC4GN61	TCC4GN60	00	
TC4GNC2	DB	0	1	↑	1	1	0	1	1	0	1	1		Gamma 4BPP TC Range C Negative
		1	1	↑	TCC4GN93	TCC4GN92	TCC4GN91	TCC4GN90	TCC4GN83	TCC4GN82	TCC4GN81	TCC4GN80	00	
		1	1	↑	TCC4GNB3	TCC4GNB2	TCC4GNB1	TCC4GNB0	TCC4GNA3	TCC4GNA2	TCC4GNA1	TCC4GNA0	00	

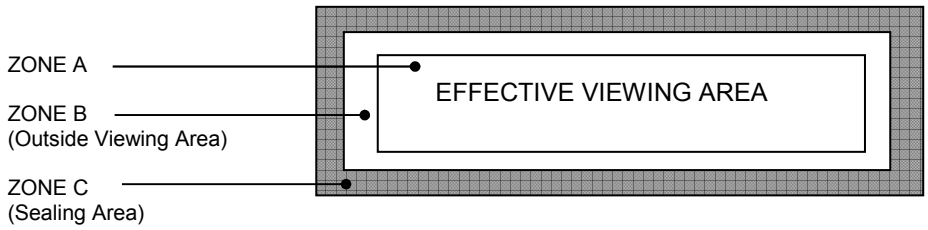
		1	1	↑	TCC4GND3	TCC4GND2	TCC4GND1	TCC4GND0	TCC4GNC3	TCC4GNC2	TCC4GNC1	TCC4GNC0	00	polarity
		1	1	↑	TCC4GNF3	TCC4GNF2	TCC4GNF1	TCC4GNF0	TCC4GNE3	TCC4GNE2	TCC4GNE1	TCC4GNE0	00	
TC4GPD1	DC	0	1	↑	1	1	0	1	1	1	0	0		
		1	1	↑	TCD4GP13	TCD4GP12	TCD4GP11	TCD4GP10	TCD4GP03	TCD4GP02	TCD4GP01	TCD4GP00	00	Gamma 4BPP
		1	1	↑	TCD4GP33	TCD4GP32	TCD4GP31	TCD4GP30	TCD4GP23	TCD4GP22	TCD4GP21	TCD4GP20	00	TC Range D
		1	1	↑	TCD4GP53	TCD4GP52	TCD4GP51	TCD4GP50	TCD4GP43	TCD4GP42	TCD4GP41	TCD4GP40	00	Positive polarity
		1	1	↑	TCD4GP73	TCD4GP72	TCD4GP71	TCD4GP70	TCD4GP63	TCD4GP62	TCD4GP61	TCD4GP60	00	
TC4GPD2	DD	0	1	↑	1	1	0	1	1	1	0	1		
		1	1	↑	TCD4GP93	TCD4GP92	TCD4GP91	TCD4GP90	TCD4GP83	TCD4GP82	TCD4GP81	TCD4GP80	00	Gamma 4BPP
		1	1	↑	TCD4GPB3	TCD4GPB2	TCD4GPB1	TCD4GPB0	TCD4GPA3	TCD4GPA2	TCD4GPA1	TCD4GPA0	00	TC Range D
		1	1	↑	TCD4GPD3	TCD4GPD2	TCD4GPD1	TCD4GPD0	TCD4GPC3	TCD4GPC2	TCD4GPC1	TCD4GPC0	00	Positive polarity
		1	1	↑	TCD4GPF3	TCD4GPF2	TCD4GPF1	TCD4GPF0	TCD4GPE3	TCD4GPE2	TCD4GPE1	TCD4GPE0	00	
TC4GND1	DE	0	1	↑	1	1	0	1	1	1	1	0		
		1	1	↑	TCD4GN13	TCD4GN12	TCD4GN11	TCD4GN10	TCD4GN03	TCD4GN02	TCD4GN01	TCD4GN00	00	Gamma 4BPP
		1	1	↑	TCD4GN33	TCD4GN32	TCD4GN31	TCD4GN30	TCD4GN23	TCD4GN22	TCD4GN21	TCD4GN20	00	TC Range D
		1	1	↑	TCD4GN53	TCD4GN52	TCD4GN51	TCD4GN50	TCD4GN43	TCD4GN42	TCD4GN41	TCD4GN40	00	Negative
		1	1	↑	TCD4GN73	TCD4GN72	TCD4GN71	TCD4GN70	TCD4GN63	TCD4GN62	TCD4GN61	TCD4GN60	00	polarity
TC4GND2	DF	0	1	↑	1	1	0	1	1	1	1	1		
		1	1	↑	TCD4GN93	TCD4GN92	TCD4GN91	TCD4GN90	TCD4GN83	TCD4GN82	TCD4GN81	TCD4GN80	00	Gamma 4BPP
		1	1	↑	TCD4GNB3	TCD4GNB2	TCD4GNB1	TCD4GNB0	TCD4GNA3	TCD4GNA2	TCD4GNA1	TCD4GNA0	00	TC Range D
		1	1	↑	TCD4GND3	TCD4GND2	TCD4GND1	TCD4GND0	TCD4GNC3	TCD4GNC2	TCD4GNC1	TCD4GNC0	00	Negative
		1	1	↑	TCD4GNF3	TCD4GNF2	TCD4GNF1	TCD4GNF0	TCD4GNE3	TCD4GNE2	TCD4GNE1	TCD4GNE0	00	polarity
TOSC	F4	0	1	↑	1	1	1	1	0	1	0	0		
		1	1	↑	0	0	0	0	0	0	0	0	00	Command for
		1	1	↑	0	1	1	0	0	1	1	1	67	MTP Autoload
		1	1	↑	1	1	1	MTPAuto	1	1	1	0	FE	Control
		1	1	↑	1	1	1	0	1	0	1	0	EA	
TCSET	F6	0	1	↑	1	1	1	1	0	1	1	0		
		1	1	↑	0	0	0	0	Crack	0	0	0	08	Command for
		1	1	↑	0	0	0	0	0	0	0	0	00	TC
		1	1	↑	0	0	0	0	0	0	0	0	00	Temperature
		1	1	↑	0	0	1	0	0	0	0	1	21	Control

10.1 Initialization code for ST7513

```
Write(COMMAND, 0xae);
Write(DATA, 0xa5);
Write(COMMAND, 0x54);
Write(DATA, 0x0e);
Write(DATA, 0x00);
Write(DATA, 0x00);
Write(DATA, 0xa5);
Write(COMMAND, 0x61);
Write(DATA, 0x8f);
Write(DATA, 0x04);
Write(DATA, 0x02);
Write(DATA, 0xa5);
Write(COMMAND, 0x62);
Write(DATA, 0x3C);
Write(DATA, 0x0b);
Write(DATA, 0x0b);
Write(DATA, 0xa5);
Write(COMMAND, 0x63);
Write(DATA, 0x17);
Write(DATA, 0x17);
Write(DATA, 0xa5);
Write(DATA, 0xa5);
Write(COMMAND, 0x12);
Write(DATA, 0xa5);
Write(COMMAND, 0x24); //mx=1
Write(DATA, 0x01);
Write(DATA, 0xa5);
Write(DATA, 0xa5);
Write(DATA, 0xa5);
Write(COMMAND, 0x1b);
Write(DATA, 0xa5);
Write(COMMAND, 0x15);
Write(DATA, 0xa5);
```

11.0 Quality Assurance

11.1 Zone Definition

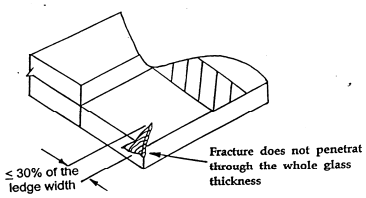


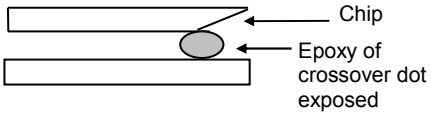
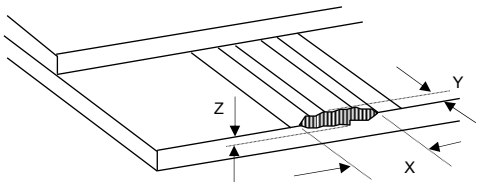
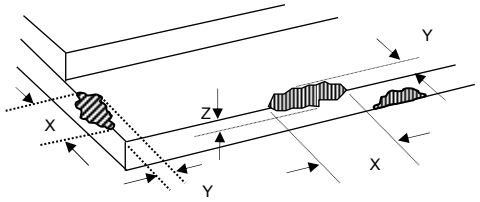
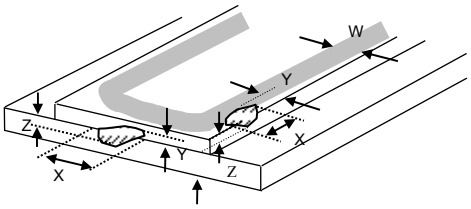
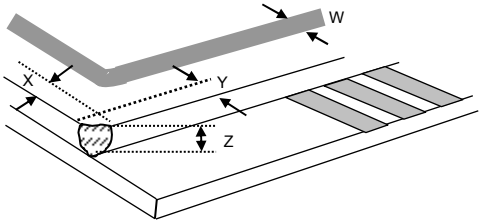
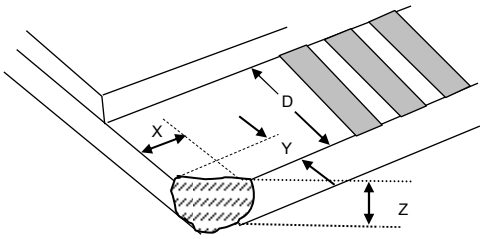
11.2 Rejection Criteria

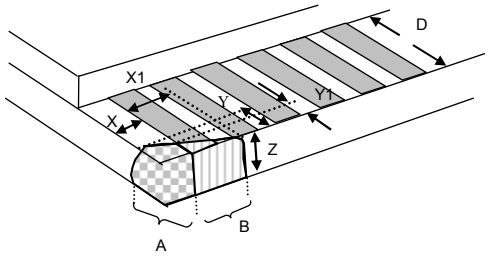
11.2.1 Dimensional Defects

Defect Category	Defect Description	Criterion	Drawing Specification
Glass Size	Dimensions of LCD, do not conform to the drawing	Reject	Refer to LCD Physical Dimension Drawing
Perimeter Seal Extension	Perimeter seal epoxy enters the effective viewing area	Reject	
End Seal Size	Size of end seal does not meet drawing specification	Reject	Refer to LCD Physical Dimension Drawing

11.2.2 Visual Defects

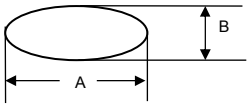
Defect Category	Defect Description	Criterion	Drawing Specification
Fracture	A type of glass breakage containing running cracks. Inspectors should attempt to remove it with fingernail. If removed, evaluate as chip	Reject – if the size is $\geq$ 30% of the contact ledge width.	

Defect Category	Defect Description	Criterion	Drawing Specification
Chip	Chip in cross over area	1) Reject - if the chip causes crossover dot to be exposed 2) Chip on outside edge of the glass plate but is greater than 50% of glass thickness at crossover dot is reject able.	
Chip	Chip in contact pad area	Accept if:- a) X ≤ 2.0mm b) Y ≤ 0.5mm c) Z disregard	
	Chip in non-contact pad area	Accept if:- a) X ≤ 6.0mm b) Y ≤ 1.0mm c) Z disregard	
	Chip in perimeter seal area	Accept if:- a) Y ≤ 1/3 of perimeter seal width (W) b) X ≤ 3.0mm c) Z disregard d) X and Y not touch crossover dot	
Corner Chip	Corner chip within seal area	Accept if:- a) X ≤ 1/3 of perimeter seal width (W) b) Y ≤ 1/3 of perimeter seal width (W) c) Z disregard	
	Corner chip not effecting contact pad / ITO	Accept if:- a) XY ≤ 4mm^2 AND b) Y ≤ D and X ≤ 2.0mm c) Z disregard	

Defect Category	Defect Description	Criterion	Drawing Specification
	Corner chip effecting contact pad / ITO	A) Accept if:- a) XY ≤ 4mm^2 AND b) Y ≤ D and X ≤ 2.0mm B) Accept if:- a) X1 ≤ 2.0mm b) Y1 ≤ 0.5mm Z disregard	
Glass flare	A thin layer of glass flare at contact area	Accept if:- a) Flare thickness ≤ ¼ W when W ≤ 3mm b) Flare thickness ≤ 1mm when W > 3mm W: Contact ledge width	
Glass burr	A rough edge(s) left along the scribing edge (i.e. along the edges of display)	Reject – if the burr cause undersize or oversize of the LCD	Refer to LCD Physical Dimension Drawing
Rainbow	Colored ring in sharp blotches observed	Reject – if 3 or more colored rings in sharp blotches of color are observed. (Limit samples should be used when applicable)	
Discoloration		Reject - if the discolorations enter the active viewing area of LCD. Color of the LCD shall follow product specification as specified in the manufacturing specification	
Air Void	LC does not fulfill the display	Reject	
Fill end contamination	Discoloration at end seal area	Reject if discoloration exceeded the baffle (for display with baffle) or viewing area (for display without baffle)	

11.2.3 Polarizer Defects

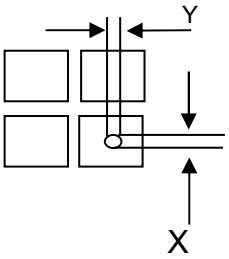
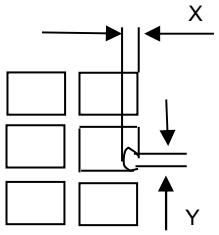
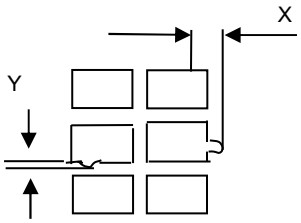
<table>
<tr><th>Defect Category</th><th>Defect Description</th><th>Criterion</th><th>Drawing Specification</th></tr>
<tr><td rowspan="5">Polarizer defect</td><td>Polarizer coverage</td><td>1- Polarizer should cover effective viewing area of display.
2- It is acceptable if perimeter seal bolder at all sides could be seen.
3- It is acceptable if polarizer attaching position meeting the tolerance mentioned in the drawing.
4- It is reject able if polarizer edge jagged and not even</td><td>Refer to LCD Physical Dimension Drawing</td></tr>
<tr><td>Polarizer Peeling / delamination</td><td>1- Reject if any edge or corner of the polarizer is lifted up or not adheres to the glass</td><td></td></tr>
<tr><td>Polarizer Scratches</td><td>1- Any scratch should be acceptable if it is not visible from viewing distance at head of position
2-Polarizer scratch in viewing area is reject able if it is visible from the specified viewing distance
3-Defect, which is visible under surface glare, should be disregard</td><td></td></tr>
<tr><td>Polarizer damage</td><td>1-Stain mark or depression in front polarizer surface should be acceptable if it is not visible from viewing distance at head on position.
2-Defect, which is visible under surface glare, should be disregard</td><td></td></tr>
<tr><td>Polarizer bubble / Foreign material</td><td>
<table>
<tr><td rowspan="2">Zone / Dimension</td><td colspan="3">Acceptable No.</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>D ≤ 0.30mm</td><td>NC</td><td>NC</td><td rowspan="4">NC if the Polarizer not lifted up/ peel off</td></tr>
<tr><td>D ≤ 0.50mm</td><td>2</td><td>NC</td></tr>
<tr><td>0.50 < D ≤ 0.60mm</td><td>1</td><td>2</td></tr>
<tr><td>D > 0.60mm</td><td>0</td><td>0</td></tr>
</table>
NC: No count
D: Mean Diameter of Defect

3 are the totally permissible numbers of bubble</td><td> 

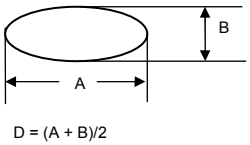
D = (A + B)/2</td></tr>
</table>

11.2.4 Electrical Test Defects

Defect Category	Defect Description	Criterion	Drawing Specification
Missing common	Part of the pattern does not light up	Reject	
Missing segment	One or few segment does not light up	Reject	
Common-common short	Common and common connected	Reject	

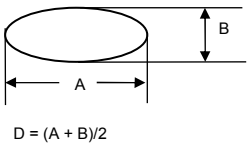
<table>
<tr><td>Segment-segment short</td><td>Segment and segment connected</td><td>Reject</td><td></td></tr>
<tr><td>Common – segment short</td><td>Common and segment connected</td><td>Reject</td><td></td></tr>
<tr><td>Wrong viewing angle</td><td>Wrong viewing angle</td><td>Reject if display viewing angle not conform to customer requirement</td><td></td></tr>
<tr><td>Metal residue</td><td>Extra spot lights up at the border of the segment.</td><td>Accept if ≤ 0.20mm (mean diameter)</td><td></td></tr>
<tr><td>Slow response</td><td>Response of the display on one side slower than the other side</td><td>Reject if it is visible at 30cm distance</td><td></td></tr>
<tr><td>Pin Hole</td><td>Pin hole / void at light up segment</td><td><table><tr><td>Zone / Dimension</td><td>Acceptable No.</td></tr><tr><td>Located inside single pixel/dot:- (X + Y)/2 ≤ 0.20mm</td><td>- 1 per pixel/dot
- 3 per display (Active Area)</td></tr><tr><td>Laid over the plural pixel/dots: (X + Y)/2 ≤ 0.20mm</td><td>- 1 per pixel/dot
- 3 per display (Active Area)</td></tr><tr><td colspan="2">(¾ or larger part of dot area has to be effective for display)</td></tr></table></td><td> 
</td></tr>
<tr><td rowspan="2">Deformed display dot</td><td>Lacked deformation</td><td>Accept if:
i) X ≤ 0.15 and
ii) Y ≤ 0.15</td><td> 
</td></tr>
<tr><td>Added deformation</td><td>Accept if:
i) X < 0.02 and
ii) Y < 0.02</td><td> 
</td></tr>
<tr><td>Reverse twist/ tilt</td><td>Segment are darker or clearer than other area of the same segment</td><td>Reject</td><td></td></tr>
<tr><td>Misalignment</td><td>Segment fatter or smaller or extra segment</td><td>Reject if > 10% of designed segment width and visible at 30cm distance</td><td></td></tr>
<tr><td>Segment Smearing</td><td>Light up segment smear</td><td>Reject</td><td></td></tr>
<tr><td>Dim segment</td><td>Display shows poor contrast at pre set voltage</td><td>Reject</td><td></td></tr>
</table>

11.2.5 Black Spot, White Spot and Foreign Material (Solid Figure)

Defect Category	Defect Description	Criterion				Drawing Specification
Black Spot, White Spot and Foreign Material	Black Spot, White Spot and Foreign Material	Zone / Dimension	Acceptable No.			 D = (A + B)/2
			A	B	C	
		D ≤ 0.10mm	NC	NC	NC	
		0.10<D ≤ 0.15mm	3	3	NC	
		0.15 < D ≤ 0.25mm	1	2	NC	
		0.25 < D ≤ 0.35mm	1	1	NC	
		D > 0.35 mm	0	0	NC	
		NC: No count D: Mean Diameter of Defect				

*Note: The 1/3 or larger parts of individual dot has to be lighted on.
The solid figure is that the defect has clear-cut outline at the optimum driving condition in both positive and negative, of which size does not change when the contrast changes.

11.2.6 Black Spot, White Spot and Foreign Material (Faded Figure)

Defect Category	Defect Description	Criterion				Drawing Specification
Black Spot, White Spot and Foreign Material	Black Spot, White Spot and Foreign Material	Zone / Dimension	Acceptable No.			 D = (A + B)/2
			A	B	C	
		D ≤ 0.60mm	NC	NC	NC	
		0.60<D ≤ 0.70mm	3		NC	
		0.70 < D ≤ 0.80mm	1		NC	
		D > 0.80 mm	0		NC	
		NC: No count D: Mean Diameter of Defect				

*Note: Faded figure means that the defects has unclear outline at the optimum driving condition in both positive and negative, of which size seems to change when the contrast changes.

11.2.7 Line Shape and Scratches

<table>
<tr><th>Defect Category</th><th>Defect Description</th><th colspan="5">Criterion</th><th>Drawing Specification</th></tr>
<tr><td rowspan="6">Line shape and scratches</td><td rowspan="6">Line shape and scratches</td><td colspan="5"></td><td rowspan="6"></td></tr>
<tr><td colspan="2">Zone /Dimension</td><td colspan="3">Acceptable No.</td></tr>
<tr><td>X</td><td>Y</td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>NC</td><td>≤ 0.03mm</td><td>NC</td><td>NC</td><td>NC</td></tr>
<tr><td>≤ 2 mm</td><td>≤ 0.05mm</td><td>1</td><td>1</td><td>NC</td></tr>
<tr><td>≤ 1 mm</td><td>≤ 0.10mm</td><td>1</td><td>2</td><td>NC</td></tr>
<tr><td>NC</td><td>≥ 0.10mm</td><td colspan="3">Due to (1) round defect</td></tr>
</table>

*Note: Length is X and Width is Y.

REMARK:

i) Total amount of spot defects including round and linear – A total of 5 permissible numbers of defects in Zone A & B including above (12.2.5), (12.2.6), (12.2.7). Regardless of number of defects, the minimum distance between individual defects have to be 5mm or larger.

ii) All the other items of inspection that are not included herein must be determined by the “Limit Standard” sample, which were occasionally set up with the mutual consent of both parties. In every case of the items set up with the Limit Standard, the Limit Standard always takes precedence over the other means of definition.

12.0 Precaution for using LCM

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling.

a) Keep the temperature within the range of use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel off or bubble.

b) Do not contact the exposed polarizer with anything harder than HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

c) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or colour fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

d) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

e) Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules.

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modification. The following should be noted.

a) Do not tamper in any way with the tabs on the metal frame.

b) Do not modify the PCB by drilling extra holes, changing its outline, moving its component or modifying its pattern.

c) Do not touch the elastomer connector, especially insert a backlight panel (for example, EL)

d) When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

e) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2 Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

a) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

b) The modules should be kept in antistatic bags or other containers to static for storage.

c) Only properly grounded soldering irons should be used.

d) If an electric screwdriver is used, it should be well grounded and shielded from commutator spark.

e) The normal static prevention measures should be observed for work clothes and working benches, the latter conductive (rubber) mat is recommended.

f) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

2.3 Soldering

a) Solder only to the I/O terminals.

b) Use only soldering irons with proper grounding and no leakage.

c) Soldering temperature: 280 °C

d) Soldering time: 3 to 4 sec

e) Use eutectic solder with resin flux fill.

f) If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.

2.4 Operation

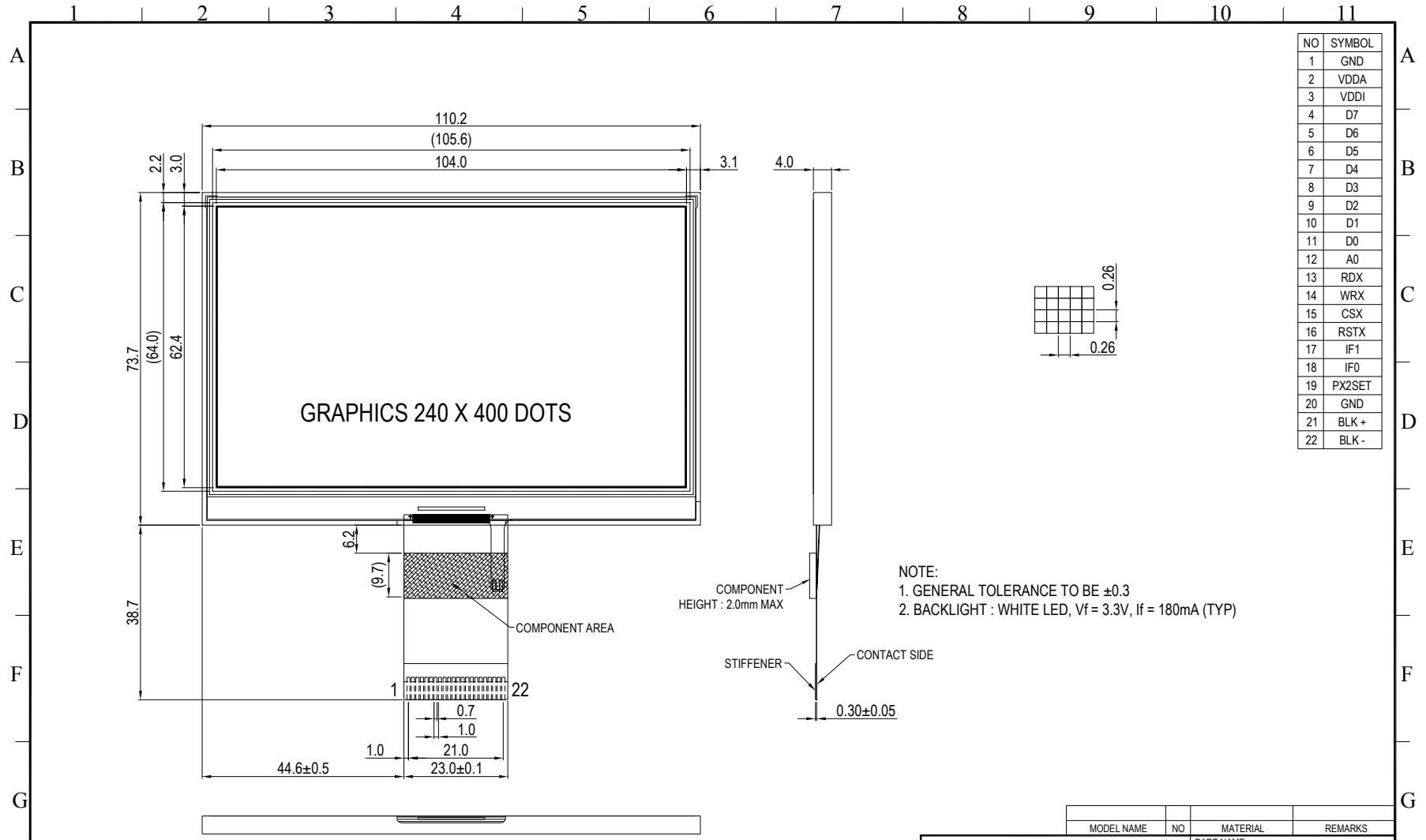
a) The contras can be adjusted by varying the LCD driving voltage V0
b) Driving voltage should be kept within specified range, excess voltage shortens display life.
c) Response time increases with decrease in temperature.
d) Display may turn black or dark blue at temperature above its operational range, this is (however not pressing on the viewing area) may cause the segments to appear "fractured".
e) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

2.5 Storage

If any fluid leaks out of the damage glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

Unless otherwise agreed between Crystal Clear Technology and customer, Crystal Clear Technology will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with Crystal Clear Technology acceptance standards, for a period of one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Crystal Clear Technology is limited to repair and/or replacement on the terms set forth above. Crystal Clear Technology will not responsible for any subsequent or consequential events.



NO	SYMBOL
1	GND
2	VDDA
3	VDDI
4	D7
5	D6
6	D5
7	D4
8	D3
9	D2
10	D1
11	D0
12	A0
13	RDX
14	WRX
15	CSX
16	RSTX
17	IF1
18	IF0
19	PX2SET
20	GND
21	BLK +
22	BLK -

NOTE:
1. GENERAL TOLERANCE TO BE ±0.3
2. BACKLIGHT : WHITE LED, Vf = 3.3V, If = 180mA (TYP)

MODEL NAME	NO	MATERIAL	REMARKS

CRYSTAL CLEAR TECHNOLOGY SDN BHD
16, JLN TP5, TMN PERINDUSTRIAN SIME UEP,
47500 SUBANG JAYA, SELANGOR DARUL EHSAN.

PART NAME: MECHANICAL SPECIFICATION

APPROVED	CHECKED	DRAWN	UNIT : MM	DRAWING NUMBER	SHEET	REV.
		AZHAR 06-10-2013	NTS	T2440W01B00	1/1	1

Crystal Clear Technology
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